# A Network-On Chip Architecture for Optimization of Area and Power with Reconfigurable Topology on Cyclone II Specific Device

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**ABSTRACT**: The Network-on-Chip (NoC) architecture enables the network topology to be reconfigured. This enables a general System-on-Chip (SoC) platform, which is currently running on the chip. The topology is configured using area- efficient topology and so it is optimised design

KEYWORDS: SOC, NOC, Area and power efficient, CMOS sensor application

### I. INTRODUCTION

Every new CMOS technology generation enables the design of larger and more complex systems on a single integrated circuit. The increasing complexity also means that design, test and production costs reach levels where large volumes must be produced for a chip to be feasible. The time it takes to get a new product to the market (time-to market) thereby also increases. This trend seems to make ASICs infeasible for the main bulk of applications the development time will simply be too long. For many applications a more general System-on-Chip (SoC) platform chip could be a viable solution. Such a SoC platform would contain many different IP-Blocks including RAMs, CPUs, DSPs, IOs, FPGAs and other coarse and fine grained programmable IP-Blocks. The communication is provided by means of a flexible communication infrastructure in the form of a Networkon-Chip (NoC). This allows the same SoC platform to be used in a wide range of different applications and thereby increases the production volume. As the same SoC platform is to be used for many different applications, the NoC must be able to support a wide range of bandwidth and Quality-of-Service (QoS) requirements. The requirements of the applications can be very different, and the NoC must therefore be very flexible. Currently, the only way to provide such flexibility is to employ a large packet-switched NoC with an over-engineered total bandwidth capacity. Such a NoC would take a significant part of the SoCs silicon area and only a fraction of its capacity is utilized by a given application. The topology switches are implemented using physical circuit-switching as found in FPGAs, to minimize the power consumption and area overhead. The motivation for inserting a configurable layer below existing NoC architectures is that physical circuit switching is far more efficient than intelligent, complex packet-switching which therefore must be avoided when possible. The communication requirement for the application is therefore used to configure a logical topology that minimizes the amount of packet-switching.

### **II HETEROGENEOUS PHYSICAL ARCHITECTURE:**

In this architecture we are using routers and topology switches separately as well as combined also taking for network nodes and so the architecture is complex



Figure 1 : Example of a complex, heterogeneous, physical architecture

Network nodes can contain a router, a topology switch, or both. Several IP-cores can be connected to the same network node, several link scan exist between network nodes, and IP-blocks can be directly connected.

The architecture is not restricted to a specific router. The only requirement is that the link width, including wires for flow-control, matches the ports on the router. In principle the communication protocol is defined by the routers and the topology switches and links act as passive circuit-switched interconnects. This means that the architecture can be used in combination with any existing router. The routers can contain Virtual Channels (VC), Quality of-Service (QoS) implementations such as TDM, queuing buffers, and can be implemented using synchronous or asynchronous circuit techniques.

### **III CMOS SENSOR APPLICATION AS BENCHMARK**

Input can be used as real-time raw video streams from the CMOS sensor board in which we can do image capturing, video processing from basic images. Tools using for this process is Quartus II, Sopc builder, NiosII



Figure 2: Overview of cyclone II DE2 BOARD

This is a basic cyclone II DE2 board for video processing which can be interfaced with extra CMOS SENSOR daughter card. The basic kit contains RS232 serial port and video input port and video output serial ports. So that implementation of video processing is possible without a LCD touch panel display in the base kit Through Synopsys tools (.i.e., Design vision, prime time) we can estimate optimised area and power of our design but can't be implemented in fpgas before chip fabrication. So in order to check our designs before fabrication we are going to quartus II and nios II software tools for estimations of optimised area and power as well as we can implement on FPGAS

### **VOPD** application building



### **VOPD Schematic**

	Holk sdram clk	OUTPUT
	reset n sys clk	OUTPUT Sys_olk
,	vga clk	
	SRAM ADDR from the Pixel Buffer[170]	DUTPUT SRAM_ADDR_from_the_Pixel_Buffer[170]
	SRAM_CE_N_from_the_Pixel_Buffer	OUTPUT SRAM_CE_N_from_the_Pixel_Buffer
	SRAM_DQ_to_and_from_the_Pixel_Buffer[150]	SRAM_DO_to_and_from_the_Pixel_Buffer[150]
	SRAM LB N from the Pixel Buffer	SRAM_LB_N_from_the_Pixel_Buffer
	SRAM OE_N_from the_Pixel_Buffer	OUTPUT SRAM_OE_N_from_the_Pixel_Buffer
	SRAM UB N from the Pixel Buffer	SRAM_UB_N_from_the_Pixel_Buffer
	SRAM WE N from the Pixel Buffer	OUTPUT SRAM_WE_N_from_the_Pixel_Buffer
	VGA BLANK from the VGA Controller	QUTPUT VGA_BLANK_from_the_VGA_Controller
	VGA B from the VGA Controller[90]	OUTPUT VGA_B_from_the_VGA_Controller[90]
	VGA G from the VGA Controller[90]	DUTPUT VGA_G_from_the_VGA_Controller[90]
	VGA HS from the VGA Controller	OUTPUT VGA_HS_from_the_VGA_Controller
	VGA R from the VGA Controller[90]	UTPUT VGA_R_from_the_VGA_Controller[90]
	VGA SYNC from the VGA Controller	OUTPUT VGA_SYNC_from_the_VGA_Controller
	VGA_VS_from_the_VGA_Controller	OUTPUT VGA_VS_from_the_VGA_Controller
	zs_addr_from_the_sdram[110]	OUTPUT       zs_addr_from_the_sdram[110]
	zs ba_from_the_sdram[10]	OUTPUT zs_ba_from_the_sdram[10]
	zs_cas_n_from_the_sdram	OUTPUT zs_cas_n_from_the_sdram
	zs_cke_from_the_sdram	OUTPUT zs_cke_from_the_sdram
	zs_cs_n_from_the_sdram	OUTPUT zs_cs_n_from_the_sdram
	zs_dq_to_and_from_the_sdram[150]	EIDIR zs_dq_to_and_from_the_sdram[150]
	zs_dqm_from_the_sdram[10]	ZS_dqm_from_the_sdram(10)
	zs_ras_n_from_the_sdram	OUTPUT zs_ras_n_from_the_sdram
	zs_we_n_from_the_sdram	OUTPUT zs_we_n_from_the_sdram
	address to the cfi flash[210]	OUTPUT address_to_the_ofi_flash[210]
	data to and from the cfi flash[70]	data_to_and_from_the_cfi_flash[70]
	read n to the cfi flash	OUTPUT read_n_to_the_cfi_flash
	select n to the cfi_flash	OUTPUT
	write n to the cfi flash	QUTPUT write_n_to_the_cfi_flash
1		1 K

**Result for SoC Generation** 

ystem Contents System Generation			
Options			
System module logic will be created in Verilog.			
Simulation. Create project simulator files. Run Sit	ulator		
Nos Il Tools			
Nos I DE			
			6
# 2013.05.15 11:04:45 (*) Running Generator Program fr			
# 2013.05.15 11:05:09 (*) Running Generator Program fr	r nos_i_cock_u		
# 2013.05.15 11:05:10 (*) Running Test Generator Progr	m for sdram		
# 2013.05.15 11:05:11 (*) Making arbitration and system			
# 2013.05.15 11:05:18 (*) Generating Quartus symbol fo	top levet nios_ii		
# 2013.05.15 11:05:18 (*) Symbol C:/altera/guartus/detai	s/proc/DE2_Zip_File_System2/hios_il.bsf	already exists, no need to regenerate	
# 2013.05.15 11:05.18 (*) Creating command-line system-generation script: C/altera/guartus/sidetalis/proc/DE2_Zip_File_System2hios_i_generation_script			
# 2013.05.15 11:05:19 (*) Running setup for HDL simula	or: modelsim		
# 2013.05.15 11:05:19 (*) Completed generation for syst	em: nios_ii.		
# 2013.05.15 11:05:19 (*) THE FOLLOWING SYSTEM ITE	IS HAVE BEEN GENERATED:		
SOPC Builder database : C:/attera/guartus/details/proc/	E2_Zip_File_System2/hios_i.ptf		
System HDL Model : C:/attera/quartus/details/proc/DE2	Zip File System2hios il.v		
System Generation Script : C:/aitera/guartus/details/pro		on_script	ſ
# 2013.05.15 11:05:19 (*) SUCCESS: SYSTEM GENERA	ION COMPLETED.		
Info: System generation was successful.			
			>
Info: cfi flash: Flash memory capacity: 4.0 MBytes (419	1994 (m. 4 m. 4)		
Info: Pixel Buffer_VGA: Video Format Conversion: 320		warning: 16-bit RCB -> 10-bit RCB	
Info: VGA_Controller: Video Output Stream: Format: 64			
) The <b>Control</b> et. Theo copy decard formation	2 400 Hall Color. To (ora) 2 0 (planes)		

## SoC Implementation results for Area of specific device

Flow Summary	
Flow Status	Successful - Fri Nov 22 06:42:31 2013
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	DE2_Zip_File_System2
Top-level Entity Name	DE2_Zip_File_System2
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	0/33,216(0%)
Total combinational functions	0/33,216(0%)
Dedicated logic registers	0/33,216(0%)
Total registers	0
Total pins	426 / 475 ( 90 % )
Total virtual pins	0
Total memory bits	0 / 483,840 ( 0 % )
Embedded Multiplier 9-bit elements	0/70(0%)
Total PLLs	0/4(0%)

## Power estimated for SoC Implementation of specific device

# PowerPlay Power Analyzer Summary

PowerPlay Power Analyzer Status	Successful - Fri Nov 22 07:02:01 2013
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	DE2_Zip_File_System2
Top-level Entity Name	DE2_Zip_File_System2
Family	Cyclone II
Device	EP2C35F672C6
Power Models	Final
Total Thermal Power Dissipation	160.87 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	80.09 mW
1/0 Thermal Power Dissipation	80.78 mW
Power Estimation Confidence	High: user provided sufficient toggle rate data

Device: EP2C35F672C6			Tatik: Floorplan Editing (Assignn 💌
-ASDO- Pin E3 / Pad 0 Bank 2 (ASDO			
-nCSO- Pinto /Pad 1 Bant 2 (nCSO			
Pin B2 / Pad 2 Bank 2 (LVDS49p/CRC_E			
Pin B3 / Pad 3 Bank 2 (L/VDS49n/CL/Block utilization: 2 of 5			
Pin E5 / Pad 4 Bank 2 (PLL3_OUTp Row			

## Chip planner





**Technology post mapping** 



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## NoC implementation results for area of specific device

## Flow Summary

Flow Status	Successful - Fri Nov 22 06:21:56 2013
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	DE2_Zip_File_System2
Top-level Entity Name	DE2_Zip_File_System2
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	4,624 / 33,216 ( 14 % )
Total combinational functions	4,142 / 33,216 ( 12 % )
Dedicated logic registers	2,813 / 33,216 ( 8 % )
Total registers	2930
Total pins	426 / 475 ( 90 % )
Total virtual pins	0
Total memory bits	75,136 / 483,840 ( 16 % )
Embedded Multiplier 9-bit elements	4/70(6%)
Total PLLs	1/4(25%)

### Power estimation for NoC implementation of specific device

PowerPlay Power Analyzer Summary	
PowerPlay Power Analyzer Status	Successful - Fri Nov 22 06:38:02 2013
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	DE2_Zip_File_System2
Top-level Entity Name	DE2_Zip_File_System2
Family	Cyclone II
Device	EP2C35F672C6
Power Models	Final
Total Thermal Power Dissipation	161.18 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	80.09 mW
I/O Thermal Power Dissipation	81.09 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

## Wizard display while connecting to niosII processor

OpenCore Plus Status	
Click Cancel to stop using OpenCore Plus IP.	
Time remaining: unlimited	
Cancel	

### Building embedded designs using nios II wizard

```
🗖 bmp.c 🛛 🗖 bmp.h
                                                               ~
  /* open the file */
  if ((fp = fopen(file, "rb")) == NULL)
  {
    printf("Error opening file %s.\n",file);
    exit(1);
  }
  /* check to see if it is a valid bitmap file */
                                                               ≣
  if (fgetc(fp)!='B' || fgetc(fp)!='M')
  {
    fclose(fp);
    printf("%s is not a bitmap file.\n",file);
    exit(1);
  }
  /* read in the width and height of the image, and the
     number of colors used; ignore the rest */
  fskip(fp,16);
  fread(&b->biWidth, sizeof(short), 1, fp);
  fskip(fp,2);
  fread(&b->biHeight,sizeof(short), 1, fp);
  fskip(fp,4);
  fread(&b->biBitCount,sizeof(short), 1, fp);
~
                                                            >
                Ш
```

Implementation of NoC using nios II



### IV CONCLUSION AND FEATURE WORK

We are using CMOS SENSOR BOARD for this application in which we are giving digital video as real time input and also we can capture image from the real time video processing.

This can be basic idea to further research to video conferencing, multimedia applications, and IP surveillance cameras

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